In The Claims:

Please amend the claims as follows:

1. (currently amended) An extended bus structure, [[~~for~~]] coupling with a control chip set via a first accelerated graphics port bus, ~~the control chip set also coupled with a central processing unit, a system memory, and a bus,~~ the extended bus structure comprising:

~~a first accelerated graphics port bus, for coupling with the control chip set;~~

a first extended bus for expanding the first accelerated graphics port bus; [[~~and~~]]

a second accelerated graphics port bus for expanding the first accelerated graphics port bus; and

a first bridge, coupled to the control chip set via the first accelerated graphics port bus and further coupled to the [[~~first~~]]second accelerated graphics port bus and the first extended bus for converting mutually and compatibly signal and data between the first and second accelerated graphics port [[~~bus~~]]buses and the first extended bus, wherein the first accelerated graphics port bus is at least expanded into the first extended bus and the first and second accelerated graphics port buses, ~~wherein the first bridge is not directly coupled to the control chip set~~.

Claims 2-3 (canceled)

4. (currently amended) The extended bus structure of claim [[~~3~~]]1, wherein the first bridge [[~~further~~]] comprises:

a main accelerated graphics port controller coupled to the first accelerated graphics port bus for compatibly receiving and transmitting data and signal thereof;

a first extended bus controller coupled to the first extended bus for compatibly receiving and transmitting data and signal thereof;

an extended accelerated graphics port controller coupled to the second accelerated graphics port bus for compatibly receiving and transmitting data and signal of the second accelerated graphics port bus; and

a flow controller coupled to the main accelerated graphics port controller, the extended accelerated graphics port controller, and the first extended bus controller for arbitrating and controlling flow direction of data and signal [[~~of~~]]into/from the main accelerated graphics port controller, the extended accelerated graphics port controller, and the first extended bus controller.

5. (currently amended) The extended bus structure of claim [[~~3~~]]4, further comprising:

a second extended bus, coupled to the first bridge to expand the [[~~second~~]]first accelerated graphics port bus; and

wherein the first bridge further comprises a second extended bus controller coupled to the flow controller and the second extended bus for compatibly receiving and transmitting data and signal of the second extended bus and the flow controller arbitrates and controls flow direction of data and signal into/from the second extended bus controller.

~~a second bridge coupled to the second accelerated graphics port bus and the second extended bus for converting mutually and compatibly data and signal of the second accelerated graphics port bus and the second extended bus~~.

6. (currently amended) The extended bus structure of claim 1 [[3]], further comprising:

a second ~~accelerated graphics port bus~~ bridge coupled to the first bridge via the second accelerated graphics port bus for expanding the first accelerated graphics port bus, the second bridge further coupled to a third accelerated graphics port bus and a third extended bus~~, wherein the first bridge compatibly converts data and signal of the first accelerated graphics port bus and the second extended bus~~.

Claims 7-9 (canceled)

10. (currently amended) A bridge converting signals between a first and second accelerated graphics port buses and a first extended bus, comprising:

a main accelerated graphics port controller coupled to [[~~a~~]]the first accelerated graphics port bus for compatibly receiving and transmitting data and signal thereof~~, wherein the first accelerated graphic port bus is for coupling with a control chip set, and the control chip set is also coupled with a central processing unit, a system memory, and a bus, wherein the main accelerated graphics port controller is coupled to the first accelerated graphics port bus but not directly coupled to the control chip set~~;

a first extended bus controller coupled to the first extended bus for compatibly receiving and transmitting data and signal thereof; [[~~and~~]]

an extended accelerated graphics port controller coupled to the second accelerated graphics port bus for compatibly receiving and transmitting data and signal of the second accelerated graphics port bus; and

a flow controller coupled [[~~to~~]]between the main and the extended accelerated graphics port ~~controller~~ controllers and the first extended bus controller for arbitrating and controlling flow direction of data and signal [[~~of~~]]into/from the main and the extended accelerated graphics port [[~~controller~~]]controllers and the first extended bus controller.

Claim 11. (canceled)

12. (currently amended) The bridge of claim 10, further comprising:

a second extended bus controller coupled to [[~~the~~]]a second extended bus and the flow controller for compatibly receiving and transmitting data and signal of the second extended bus, wherein the flow controller arbitrates and controls flow direction of data and signal ~~of the main accelerated graphics port controller, the first extended bus controller, and~~ into/from the second extended bus controller.

Claims 13-15 (canceled)